# A Magnetic Power and Communication Interface for a CMOS Integrated Circuit

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*Abstract*—**Bulk CMOS integrated circuits which receive power and perform all I/O functions exclusively by means of inductive coupling have been demonstrated. Both layers of metal in a conventional two-level-metal 3-μm p-well technology were used to construct on-chip planar coils for sensing and perturbing externally generated magnetic fields in the 100-kHz to 10-MHz regime. The optimal design uses few, rather than many, coil turns operated at high frequency. The power delivered to one test chip was 0.9 mW at 3 V while a second test chip demonstrated inductive low-power bidirectional communication.**

## I. Introduction

In this paper, we demonstrate the feasibility of "pinless" chips (I/O and power) fabricated in conventional bulk CMOS technology. Applications for pinless chips include smart cards [1] and tags [2], biomedical implants (see, for instance, [3]–[6]), and microsensor interfaces [7]. From among the numerous possible phenomena for coupling, including optical, magnetostatic [8], electrostatic, millimeter waves [9], electron beams [10], etc., we chose to examine inductive coupling [11]–[14]. By restricting the technology to bulk CMOS we immediately acquire significant reliability and cost advantages over more exotic technologies. On the other hand, some tasks become more difficult. Four concerns dominate the design process: 1) the lack of thick metal for constructing high-quality inductors; 2) latch-up hazards in a design without solid power supplies and ground planes; 3) the lack of good on-chip time or voltage references; and 4) the design of robust analog circuitry to accommodate noisy current-starved power supplies. The interfaces we demonstrate have significantly less bandwidth than conventional hard-wired interfaces.

Unlike magnetocouplers [15], which detect small fields with specialized devices and require substantial amounts of power, we rely on large coil-shaped antennas fabricated out of first- and second-layer metal. These coils encircle the chip in the area usually used for bonding pads. Section II discusses the theory of these antennas and the counter-intuitive result that few, rather than many, turns are optimal. In Section III, we discuss an experimental chip that demonstrates a delivery of about 1 mW of power at 3 V to an isolated CMOS die. In Section IV, we discuss a second chip which demonstrates two-ways pinless communication utilizing a very low-power on-chip transmission technique.

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## II. Inductive Coupling

A typical integrated circuit is significantly smaller than the wavelength of an electromagnetic signal at RF frequencies. This means that highly directional antennas cannot be built on chip and also that we can use quasi-static approximations. In our experiments, we use a small external coil to couple to an on-chip aluminum coil. The inductive coupling problem can be subdivided into two parts. The first part is the magnetostatic fields problem of discovering the mutual inductance between an external loop antenna and the on-chip coil. The second half of the problem is in the circuit domain, where the key issues are the proper consideration of circuit parasitics and the optimization of circuit parameters such as the excitation frequency and number of turns of the on-chip coil. We examine these tasks in order.

### A. Mutual Inductance

The open-circuit voltage $v_2(t)$ induced on the on-chip coil as a function of the current $i_1(t)$ in the off-chip coil is given by

$$v_2(t) = -n_1 n_2 M \frac{di_1(t)}{dt} \tag{1}$$

where $n_1$ is the number of turns of the external coil, $n_2$ is the number of turns of the on-chip coil, and $M$ is the mutual inductance between one turn of each coil. From (1), we see that the induced voltage is increased by operating the transmitter at higher frequencies. Equation (1) seems to indicate that increasing the number of turns of the on-chip coil $n_2$ is also beneficial, but we will see that this is actually not so because of the effect of circuit parasitics.

The single-coil mutual inductance $M$ can be calculated for a given coil geometry using the Biot–Savart law applied to the off-chip coil and Faraday's law applied to the on-chip coil [11], [13].

A key point is that, at the RF frequencies considered, the magnetic field penetrates the bulk CMOS chip with negligible attenuation and eddy currents. This conclusion is valid only because an epitaxial process was not used. A low-resistance substrate, as is sometimes used for latch-up suppression, would have the detrimental property of partially screening the magnetic field. Unfortunately, not using an epilayer makes latch-up considerations more serious. Screening will become a problem when the skin depth $\delta = (2/\sigma\omega\mu_0)^{1/2}$ becomes comparable to the substrate thickness, where $\omega$ is the frequency of the experiment, $\sigma$ is the substrate conductivity, and $\mu_0$ is the permeability of vacuum.

### B. A Circuit Model of the Coil

A circuit model for the inductive coupling system is illustrated in Fig. 1. Since the external coil is conventional, we concentrate on the on-chip coil. Large integrated coils have a small self-inductance and a substantial distributed series resistance. There are three types of distributed capacitance. Plate and fringing capacitances exist between the coil and the conducting substrate and there is a coupling capacitance between successive turns of the coil. (While the substrate is not conductive enough to provide magnetic shielding, it is sufficiently conductive to terminate the electric field lines.) There is also the typically large capacitive load of the on-chip circuitry. Simulations of multisection models

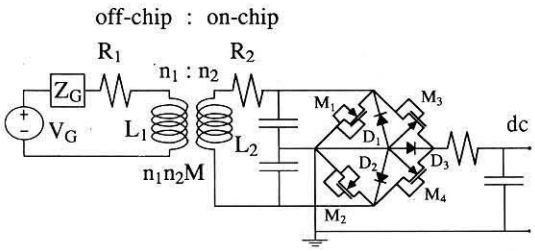



Fig. 1. Schematic of the on-chip bridge rectifier and coupling system used to produce dc power from an externally generated magnetic field. The key elements of the inductive coupling system are the transformer, resistor $R_2$, and capacitor.

show that a lumped model, as in Fig. 1, with a single transformer, inductor, resistor, and capacitor yields sufficiently accurate results. The mutual inductance is $n_1 n_2 M$.

We model the external circuitry by an external inductance $L_1$, resistance $R_1$, Thevenin impedance $Z_G(s)$, and generator voltage $V_G(s)$, where $s$ is complex frequency. The Thevenin source impedance includes the generator impedance and a tuning capacitor. The load admittance is $Y_L(s)$. A simplified expression for the voltage transfer function $G(s)$, from off-chip to on-chip, is

$$G(s) = \frac{V_L(s)}{V_G(s)} = \frac{sn_1n_2M}{(Z_G(s)+R_1+sL_1)(1+R_2Y_L(s)+sR_2C+sL_2Y_L(s)+s^2L_2C)} \quad (2)$$

where $V_L(s)$ is the voltage across the load. Because both the mutual inductance and on-chip coil currents are small, the voltage induced in the off-chip coil by currents in the on-chip coil is neglected. If we single out the key parameters in (2), and evaluate at $s = j\omega$, we find

$$G(j\omega) \propto \frac{j\omega n_1 n_2 M}{1 + j\omega R_2 C + \cdots}. \quad (3)$$

Our objective is to design an optimal on-chip coil geometry. The free variables are the excitation frequency $\omega$ and the width of each on-chip turn. We assume that each turn is identical and that all turns of the on-chip "coil" occupy an annulus of total width $t$ around the outside of a square chip with sides of length $d$. For the purposes of optimization, we further assume that the area (cost) of the coil, approximately $4td$, is fixed. The on-chip circuit parameters $L_2, R_2, C$, etc., from (2) and (3), must be translated into geometrical IC design variables, such as $n_2$, the coil width, and the coil area.

The length of the on-chip coil is approximately $4dn_2$, the width approximately $t/n_2$, and we may neglect the inter-coil spacing. For a metal of sheet resistance $\rho_s$, the resistance of an on-chip coil is approximately

$$R_2 = 4\rho_s n_2^2 d/t \quad (4)$$

and the inductance is proportional to $n_2^2 d$. The inter-coil capacitance is unimportant when compared to the plate and fringing capacitances. The latter two are approximated by a parallel-plate capacitor to the substrate of area $4td$ and capacitance per unit area $C_{ox}$. Because the coil capacitance is distributed, its effect is halved. We have

$$C = 2tdC_{ox}. \quad (5)$$

This model is supported by experiment [11], [13]. Combining (3)–(5), we find that the time constant $R_2C$ in (3) is given by

$$R_2C = 8\rho_s n_2^2 d^2 C_{ox}. \quad (6)$$

There are three key points: 1) the resistance $R_2$ grows quadratically with the number of turns $n_2$ while $C$ is independent of $n_2$; 2) there is a low-frequency fall-off of the voltage transfer function due to the frequency dependence of inductive coupling (the numerators of (2) and (3)); and 3) the voltage transfer function falls off at high frequency due to the on-chip $R_2C$ pole, given by (6). For fixed chip and coil areas, this time constant increases quadratically in $n_2$. Assuming that the off-chip coil circuitry is correctly designed, the optimization of the on-chip parameters calls for a few wide turns excited at high frequency. Decreasing $n_2$ by a factor of 2 decreases the on-chip coil resistance by a factor of 4, allowing a fourfold increase in the driving frequency and a net performance improvement of a factor of 2. This procedure is effective until several hundred megahertz, above which inductive poles become significant. One major disadvantage of conventional MOS technology is that large on-chip coils are heavily damped. The unloaded $Q$ of a coil is given by $Q = G\sqrt{L/C}$, where $G = 1/R_2$ is the conductance of the coil. For the CMOS process we used, $Q \approx 0.7/n_2 d$, where $d$ is measured in centimeters. Except for very small values of $n_2$ or very small coils (such as those used in microwave integrated circuits), integrated coils are overdamped.

## III. Power Delivery

The power delivery experiment was performed with two-level-metal bulk 3-$\mu$m p-well CMOS technology. The on-chip circuitry consisted of a 30-turn coil, a bridge rectifier, a filter resistor, and a filter capacitor. The bridge rectifier was built of n-channel MOSFET's tied in a diode configuration, as illustrated in Fig. 1. Note the grounded body contacts in the p-well and the source/drain-to-well diodes $D_1$, $D_2$, and $D_3$. It is inevitable that $D_1$ and $D_2$ be intermittently forward biased in the operation of the rectifier and, indeed, these p-n junctions provide some of the rectification since they are in parallel with $M_1$ and $M_2$. The obvious latch-up hazard thus created is addressed by keeping the bridge far from any $p^+$ active area. No latch-up problems were observed on any of the chips. It is also worth noting that, when driven by the transformer, the thresholds of $M_1$ and $M_2$ are reduced because their sources go below ground, the potential of the body contact. This problem is familiar from the design of substrate charge pumps.

A photomicrograph of the test chip is shown in Fig. 2. In the power delivery experiment a field of 20 G (0.02 T) was used to induce an ac voltage on the integrated power coil. Because of fabrication difficulties, the integrated filter capacitor was cut out of the circuit. Fig. 3(a) illustrates the power supply output voltage without a load and, in Fig. 3(b), a discrete 100-pF capacitor was substituted for the faulty on-chip capacitor and placed in parallel with a 10-k$\Omega$ load resistor. The coil occupied an area of 4.4 $\times$ 7.5 mm$^2$ and the width of each trace was 5 $\mu$m. Calculated worst-case circuit parameters for this coil were $L = 24$ $\mu$H, $C = 96$ pF, and $R = 10$ k$\Omega$, leading to an on-chip $RC$ pole near 300 kHz. The actual results were much better and the tests were performed at 980 kHz. The on-chip inductance at 300 kHz only has an impedance of $j24$, making it negligible relative to the series resistance. This experiment was designed before the optimization

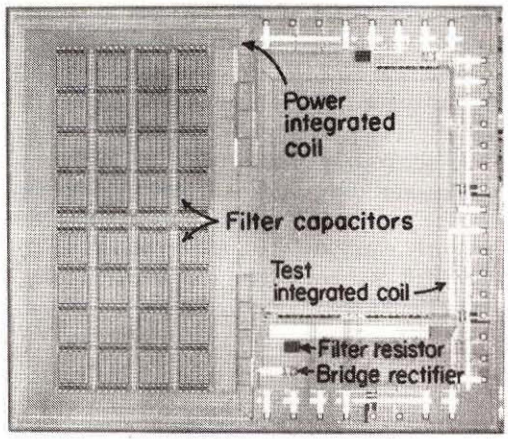
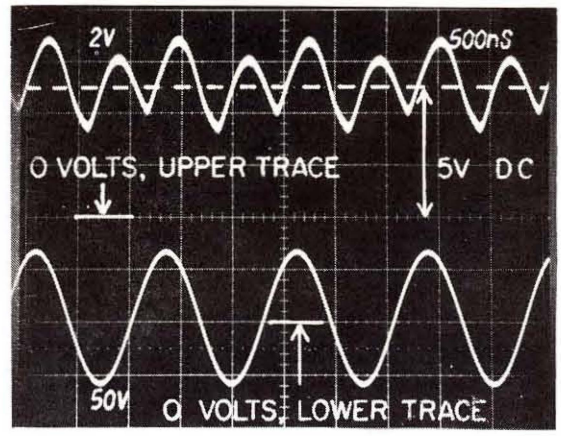
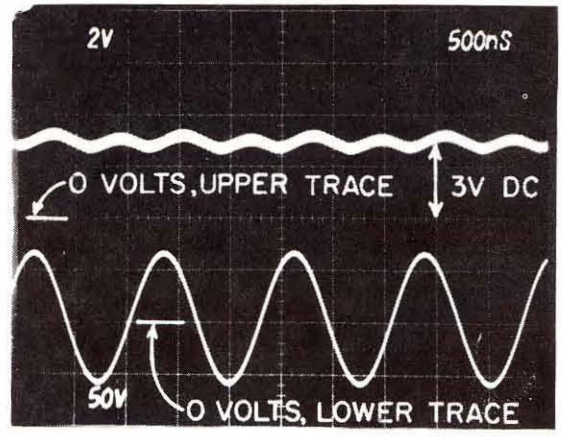



Fig. 2. Photomicrograph of the power subsystem test chip.




(a)




(b)

Fig. 3. Oscillographs of the on-chip power supply voltage. The upper traces are the on-chip voltage and the lower traces are the voltages at the off-chip generator. (a) Five-volts dc was developed into an open circuit and (b) 3 V into a load of 10 kΩ in parallel with 100 pF.

results were understood. Nevertheless, the power supply output was 3 V into 10 kΩ, or about 0.9 mW, which is more than sufficient to drive low-power CMOS circuitry at modest speeds. The power transmission efficiency was 0.05 percent. The same experiment with an optimized on-chip coil would have an efficiency near 1 percent.

## IV. The Data Transceiver

A second CMOS chip in the same technology was fabricated in order to demonstrate bidirectional data communication. A microphotograph of this chip, seen in Fig. 4, shows the two coils used for communication. In order to clearly demonstrate the capabilities of the magnetic interface, circuitry was included to perform the functions of a simple card key. In operation, a stream of data is received by the chip, encrypted, and re-transmitted. The encryption algorithm is performed by a look-up table which produces an output based on each group of three inputs. The look-up table is implemented on-chip in a PLA. Two-phase nonoverlapping clocks and power were supplied to the test chip in a conventional way to simplify the experiment. (Since it is difficult to generate a precise on-chip frequency reference, in a system one might let the chip free-run on an internally generated clock, using, for instance, a ring oscillator, and design the external circuitry to phase-lock to "local chip time" in order to provide synchronized communication. This technique was not demonstrated.) During operation, the chip was located in a pair of ferrite yokes with a 1-mm gap.

### A. Receiver

The schematic for the on-chip receiver is illustrated in Fig. 5. The chip input is an amplitude-modulated magnetic field; the voltage on the external coil is seen in the top trace of Fig. 6. The carrier frequency is 1 MHz and ten turns are used in the receiver coil. The receiver coil occupied an area of $4 \times 6.7$ mm$^2$ and each trace was 45 $\mu$m wide. Calculated worst-case circuit parameters for this coil were $L = 3$ $\mu$H, $C = 260$ pF, and $R = 360$ Ω, leading to an on-chip $RC$ pole near 3.5 MHz. Note that this coil, which occupies roughly the same area as the power coil, has a factor of 3 fewer turns but can be used at over ten times the frequency. The measured resistance, 210 Ω, was much lower than the calculated worst-case resistance for the process. At 3.5 MHz the reactance of the inductor is still only a few percent of its resistance. The receiver detects the presence of the externally

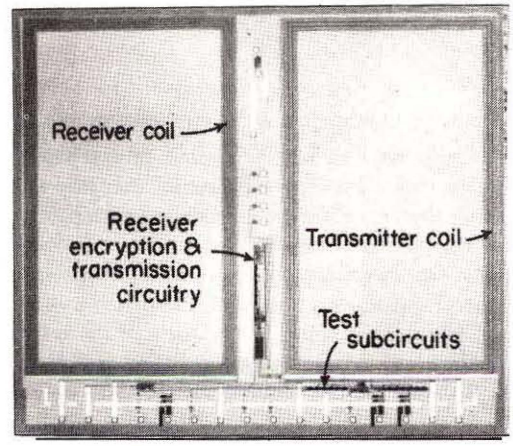



Fig. 4. Photomicrograph of the communication subsystem test chip showing the transmitter and receiver circuitry.

generated field by discharging, on $\phi_2$, the node which was precharged on $\phi_1$. Note that this simple technique would not have worked in the presence of strong light due to leakage currents. The experimentally verified robustness of this simple single-ended technique attests to the fact that on-chip noise generated by the strong fields was not a problem.

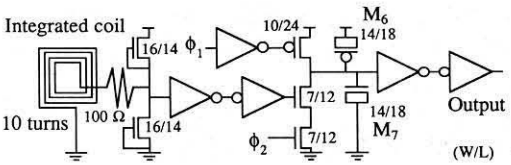



Fig. 5. Schematic of the single-ended on-chip receiver circuitry. When an externally generated signal is present, the gates of transistors $M_6$ and $M_7$ are discharged on $\phi_2$ high.

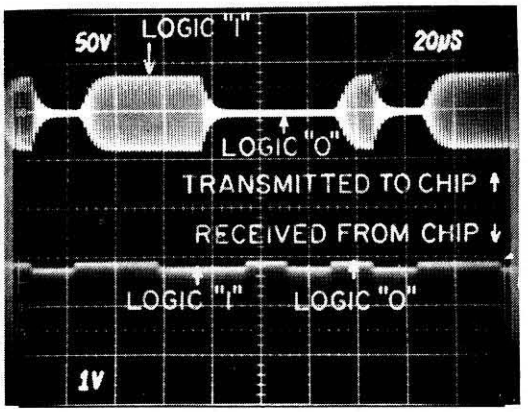



Fig. 6. Oscillograph of signals transmitted to and received from the communication test chip. An AM-modulated external signal is correctly detected on-chip, encrypted, and re-transmitted.

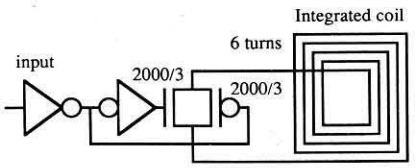



Fig. 7. Schematic of the on-chip transmission circuitry. The pass gate modulates the load on the integrated coil.

### B. Transmitter

The transmission of signals from the CMOS chip was the greatest challenge because of the limited power available and poor on-chip dc-to-RF conversion efficiency (because of the poor coil $Q$). Rather than generate the RF power on-chip, we chose to generate the RF carrier externally and modulate it on-chip. The scheme is most simply conceptualized in terms of transformers. If one views the transformer primary as the off-chip coil and the secondary as the on-chip coil, a modulation of the resistive load on the secondary will be seen at the primary as a time-varying impedance. Because the technique parametrically up-converts a low-frequency modulation into high-frequency sidebands, the received off-chip signal power can be many times larger than the power used to drive the on-chip time-varying impedance. In our implementation, this scheme used only 11 $\mu$W of on-chip power, at 50 kBd, to produce an off-chip signal of several milliwatts.

The schematic for the on-chip transmitter is shown in Fig. 7. In essence, it is just a pass gate connected to the coil. It is either closed (about 80 Ω) or open circuited. The pass gate consisted of parallel p- and n-channel transistors of drawn dimensions 2000 $\mu$m/3 $\mu$m. The six-turn transmitter coil occupies an area of roughly $4 \times 6.7$ mm$^2$ and each trace is 75 $\mu$m wide. Calculated worst-case circuit parameters for this coil were $L = 1$ $\mu$H, $C = 260$ pF, and $R = 130$ Ω (measured was 80 Ω), leading to a calculated on-chip $RC$ pole near 10 MHz. In operation, an 18-MHz sinusoidal signal was applied to the external coil and AM modulated by the action of the chip. A 4-percent modulation was achieved. Fig. 6 illustrates the correct operation of the transceiver chip. The upper trace illustrates the 1-MHz AM input signal. The pinless chip decodes the repetitive 11100010 pattern. The lower trace shows the properly encrypted data transmitted from the chip, a repetitive 00110101 pattern. The crosstalk from the off-chip transmitter was subtracted off electronically.

## V. Conclusions

All of the major components of pinless IC transceiver technology using conventional CMOS have been successfull demonstrated. The range of the power, receiver, and transmitter circuitry are easily extendable by using larger external fields and higher frequencies. In addition, the signal power in the sidebands received by the external circuitry is actually quite large, on the order of milliwatts, and a sophisticated external receiver would substantially increase its range.

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